L1: Entry 2 of 3 File: USPT Jul 4, 2000

DOCUMENT-IDENTIFIER: US 6085334 A
TITLE: Method and apparatus for testing an integrated memory device

Abstract Text (1):
A method of memory array testing that detects defects which are sensitive to environmental conditions. A repair signature is generated reflecting the repair state of the memory. A memory device is rejected if there is a change in the repair signature of the memory array over the operating range of the device. In one embodiment, an integrated circuit includes a memory array, spare memory elements for repairing defective locations of the memory array, a built-in self-test (BIST) circuit for detecting faults in the memory array, a built-in self-repair (BISR) circuit for causing the failed memory location of the memory array to be replaced with a spare memory element, and a signature generator where the signature is based on a compression of addresses corresponding to failed memory locations, wherein the signature is used to determine that a repair result of the memory array is invariant over different environmental conditions.

Detailed Description Text (11):
BISR monitoring circuit 31 includes error qualifier 38 and signature generator 32. Address generator 36 provides row address information to error qualifier 38. The row address information is the portion of the address identifying the row of the address under test. Error qualifier 38 also receives pass/fail information from data compare 34. On receipt of a fail indicator, error qualifier 38 compares the row address received from address generator 36 to a fail history of memory array 40. If there is a match, error qualifier 38 ignores the fail indication by negating the QFAIL signal. However, if there is no match detected, error qualifier 38 asserts the signal QFAIL, which indicates a first failure of this row. QFAIL is provided to signature generator 32, which creates a repair signature, where the repair signature is based on a compression of those rows which resulted in assertion of QFAIL. The repair signature is initialized to a start value and is thereafter updated each time QFAIL is asserted during BIST/BISR operation. The repair signature reflects the repair state of memory array 40 at completion of BIST/BISR operation. The repair state is a characteristic of the defective rows replaced during this repair cycle. The repair signature is a surrogate of the repair state of memory 41.

Detailed Description Text (15):
BIST 30 provides a DONE signal upon completion of testing and repair, a REJECT/ACCEPT indicator of the success of BIST/BISR testing and repairing, and a repair signature (REPAIR SIGNATURE). In one embodiment, REPAIR SIGNATURE is a serial output of BISR monitoring circuit 31. In an alternate embodiment, REPAIR SIGNATURE is a multiple bit signal provided in parallel on multiple conductors.

Detailed Description Text (20):
Referring again to FIG. 1, signature generator 32 receives a QFAIL signal from error qualifier 38. Signature generator 32 then generates a repair signature, which is a surrogate representation of the repair state of memory 41. The repair state describes which row addresses failed and were replaced. The repair state is effectively mapped into the signature, which is then used to check for changes in the repair state. Any change in the signature indicates a change in the repair

state, i.e. a change in the replacement of rows in memory 41. In one embodiment, the mapping of repair state into a signature incorporates a generation scheme that provides a sequence of unique, nonrepeating values sufficient for correspondence with the entire repair state space. There are many ways to implement a signature generator; the implementation selection is based on design criteria, such as the risk of aliasing, and the cost of implementation. For example, where the signature is generated as a function only of the QFAIL signal, such as by use of a counter, there is a risk of aliasing. This risk is introduced as the QFAIL indicates that a fail occurred, but the signature generation does not consider which address failed. In contrast, when the signature is generated as a function of the failing row address, such as by use of an accumulator, the risk of aliasing is reduced, but the cost of implementation is increased. The latter method reduces the risk of aliasing as the signature now considers more specific information, i.e. the failing row address.

Detailed Description Text (21):
In one embodiment, signature generator 32 of FIG. 1 is implemented by a counter, and the signature generated is a function of QFAIL. The counter may be a binary counter, a linear feedback shift register, gray code counter, or any other circuitry for generating a sequence of non-repeating values over a defined space. The counter is first initialized to a known value, and incremented on each occurrence of QFAIL. Upon completion of BIST testing the repair signature is available from signature generator 32 on a bus as a multiple bit signature. Alternate embodiments may output the signature in a serial manner.

Detailed Description Text (23):
operations in response to assertion of the QFAIL signal. Accumulator 65 receives a reset signal for initialization to a known value. Accumulator 65 receives a current row address of a row under test. QFAIL is provided to accumulator 65 by error qualifier 38. Assertion of QFAIL instructs accumulator 65 to process the received current row address with the accumulated value. Upon completion of BIST testing, accumulator 65 receives an asserted shift enable signal instructing accumulator 65 to serially shift the accumulated value out as the repair signature. A shift clock is provided to accumulator 65 for output control of the repair signature. Alternate embodiments may output the signature in a parallel manner via an output bus or other parallel communication means.

Detailed Description Text (24):
During production, the repair signature will be captured on the test equipment and may be tracked throughout the device's test. Typically, the test equipment will compare a first signature with a second signature to see if there has been a change. When a signature changes due to environmental conditions, such as voltage or temperature change, the device is rejected.

Detailed Description Text (26):
Processing flow continues to block 72, where the BIST 30 test cycle and BISR monitoring circuit 31 repair cycle is run. BIST 30 testing is done to detect defects in memory 41, BISR monitoring circuit 31 and BISR circuit 39 performs repair of the defective memory elements. During BIST testing, a predetermined pattern of operations is applied to memory array 40. A typical pattern will include a series of read and write operations performed on memory array 40 to detect defects in operation of memory array 40. BIST 30 generates an address for testing and then performs a sequence of read/write operations. Output data comparison checks that the data in memory array 40 is valid for the sequence of operations. When the data comparison fails, the error is qualified according to row address and a repair signature is generated in block 74. The first repair signature generated is based on the failed memory locations found in the first BIST/BISR test cycle. Processing flow continues to block 76 where the signature is stored in external test equipment. Note that the signature may be processed externally by an ATE or internally within the the integrated circuit.

Detailed Description Text (27):
At block 78, a second environmental condition is set. The second environmental condition may change multiple conditions or may only change one condition. Processing flow continues to block 80 where BIST/BISR testing and repair is performed once again to detect and repair defects. At the completion of this second BIST/BISR testing and repair cycle, a second repair signature is generated to indicate the failed memory locations discovered during the second BIST/BISR testing and repair cycle. At decision block 83 the first signature is compared to the second signature. Decision block 83 determines if there is a change in the signature. If there is a change in the signature, then the memory is rejected at block 84. If there is no change in the signature, then testing continues at block 86. If the two signatures are the same, testing continues and may include the testing of other modules or a return to block 78 to set another environmental condition.

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